

HLS Contrast Stretch 1.0 IP Core User Guide

Revised June 21, 2018; Author Ciprian Hegbeli

1 Introduction

This user guide describes the Digilent Contrast Enhancement Intellectual Property. This IP interfaces to both the Axi-Lite and Axi-Stream in order to process a video stream and control the resolution and the contrast factor.

2 Features

- Axi-Stream 24-bit video input and output
- Axi-Lite interface for contrast and resolution control
- Resolution supported: up to 1920x1080/60Hz (clock: 148.5 MHz)
- Contrast adjustment based on programmable minimum and maximum thresholds

3 Performance

The IP has been written in HLS with a target clock frequency of 150 MHz (6.67 ns) for a maximum resolution of 1920x1080. The maximum latency is at 2101693 ns with an initiation interval of 2101682 ns which is approximately one frame. The latency and initiation interval are scaled with the input resolution, meaning that a lower resolution the latency will also be lower.

4 Usage

The IP has been initially designed for a xc7z020clg400-1 target device, the resource usage for this FPGA are illustrated in

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Axi-Lite Axi-Stream
Provided with core	
Design files	C++
Simulation model	HLS Simulation
Constraints file	XDC
Software driver	Automatically generated
Tested design flows	
Design entry	Vivado™ Design Suite 2017.4
Synthesis	Vivado Synthesis 2017.4

Name	BRAM-18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	8
FIFO	0	-	125	572
Instance	0	9	2969	4003
Memory	-	-	-	-
Multiplexer	-	-	-	-
Register	-	-	-	-
Total	0	9	3094	4583
Utilization(%)	0	4	2	8

Table 1 FPGA usage

5 Overview

The IP core has been written entirely in Vivado HLS by using the HLS Video Library provided by Xilinx and a custom contrast enhancement function written by the author. The enhancement is done by contrast stretching based on the minimum and maximum thresholds in absolute value. Thresholds and resolution are programmable using AXI-Lite.

5.1 Processing

The input format for the image/video stream is the Axi-stream interface which can accept 24 bits of RGB data (8 bit/color) respecting the Xilinx video format. Before the actual contrast enhancement, the input stream is converted in to a matrix format with de height and width corresponding to the resolution of the input image, this is done using the HLS Video Library function *AXIvideo2cvMat*. The obtained matrix is the RGB color space, to be able to change the contrast value without effecting the other components of the image a different color space hade to be chosen; based on the functions of the HLS Video Library the YCbCr color space has been chosen. Conversion from RGB to YCbCr is done using the *CvtColor* provided by the video library.

Once the contrast processing has been finished the image must be converted back to RGB color space and outputted to the Axi-Stream interface. The output Axi-Stream interface has the same format as the input Axi-Stream interface.

5.2 Contrast stretch

This IP core performs contrast enhancement by using a simple linear contrast stretching algorithm which will set the every below the chosen minimum threshold to 0 and everything above the maximum threshold to 255, thus the histogram of the image is stretched. For a graphic representation of the algorithm please refer to the following figure.

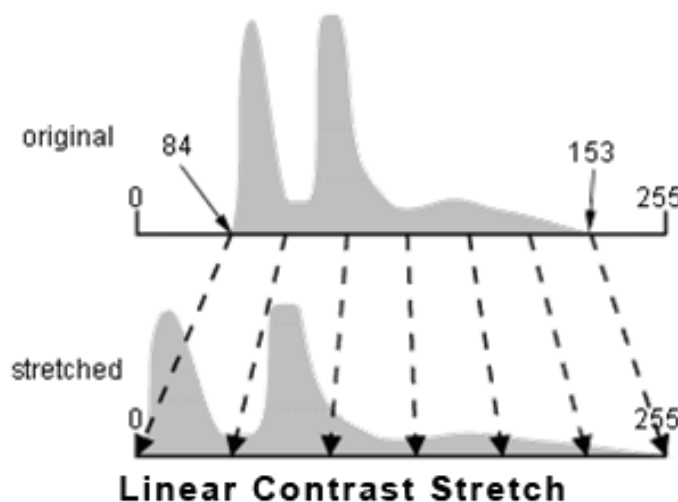


Figure 1. Contrast enhancement

Mathematically the function can be express by the following equation.

$$f(x) = \begin{cases} 0, & src.cont < min \\ \frac{(src.cont - min)}{(max - min)} * 255, & src.cont \in [min; max] \\ 255, & src.cont > max \end{cases}$$

5.3 HLS directives

The used directives for this IP core have been added to the source files, for further information on how they work and how to use them please refer to UG902: High-Level Synthesis by Xilinx.

5.4 Axi-Lite

The Axi-Lite interface is defined using HLS and controls three input variables of the main contrast stretching function. Using this interface, the user can change the resolution of both the input and the output image to a maximum of 1920x1080 and the desired contrast thresholds. Access to these parameters is provided via the automatically generated software driver, which respects the format of software drivers provided by Xilinx.

To change the minimum and the maximum thresholds, the function `XHls_contrast_stretch_Set_min` and `XHls_contrast_stretch_CSet_max` must be called.

6 Port Descriptions

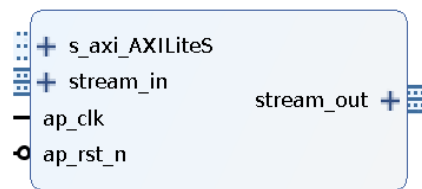


Figure 2 HLS Contrast Stretch IP core

Signal Name	Interface	Signal Type	Init State	Description
Ap_rst_n	-	I	N/A	Asynchronous reset for the core
ap_clk	-	I	N/A	Clock for the IP core, used for Stream in/output and Axi-Lite
s_axi_AXILiteS*	Axi-Lite	I	N/A	Axi-Lite interface used to configure height, width and contrast thresholds
stream_in	Axi-Stream	I	N/A	Input video stream on 24 bits, using Xilinx video format
stream_out	Axi-Stream	O	N/A	Output video stream on 24 bits, using Xilinx video format

Table 2. Port descriptions.

7 Designing with the core

7.1 Customization

The currently IP core has been packaged for a maximum frequency of 150 MHz and a maximum resolution of 1920x1080 designed for a Zynq xc7z020clg400-1 device. For customization and further changes please create a HLS project and import all the files provided in the hls_src folder of the IP.

8 References

The following document provides additional information on the subjects discussed:

1. Xilinx Inc., UG902: High-Level Synthesis, v2017.4, February 2, 2018.