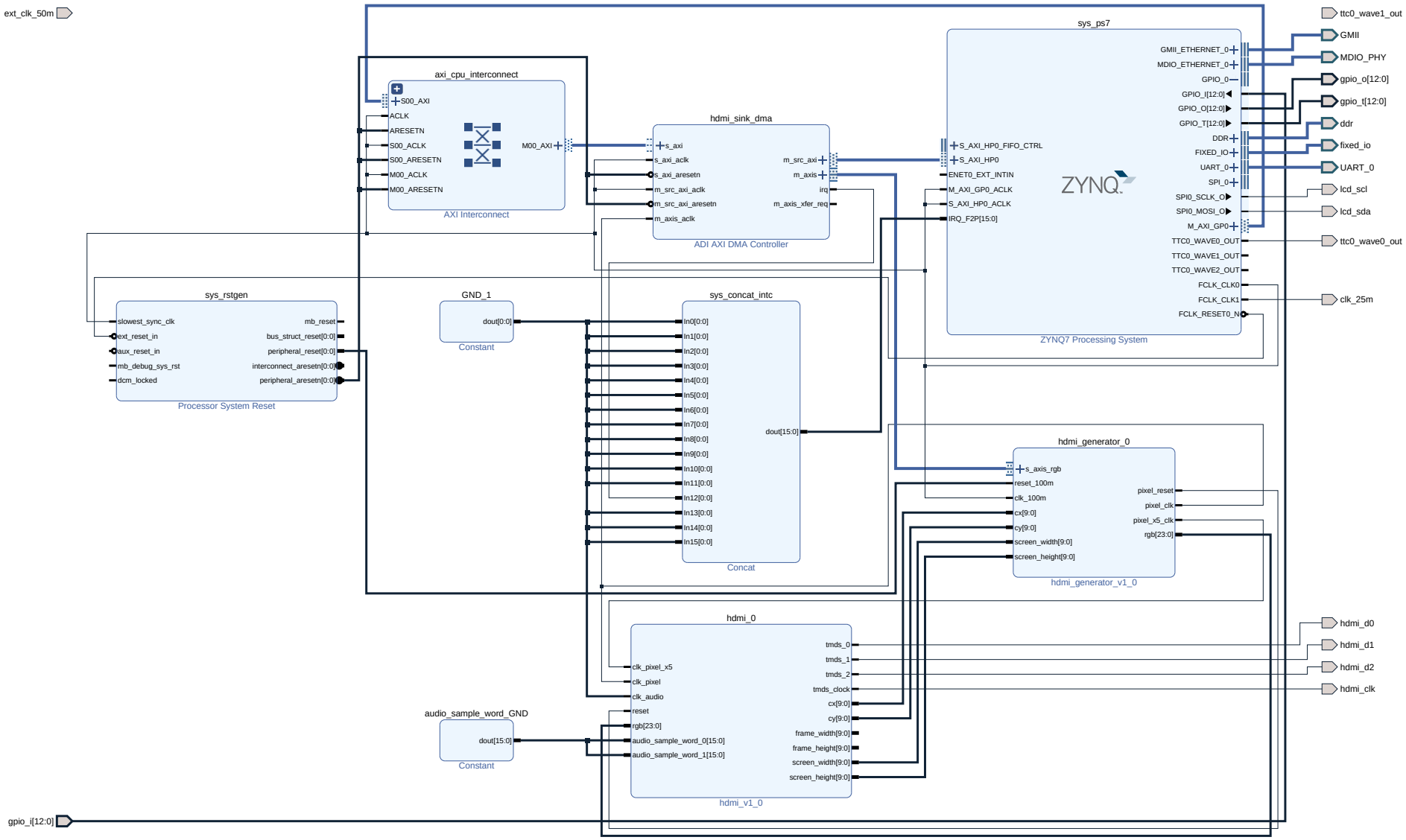
ext_clk_50m
axi_cpu_interconnect
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M00_AXI
AXI Interconnect
hdmi_sink_dma
s_axi
s_axi_aclk
s_axi_aresetn
m_src_axi_aclk
m_src_axi_aresetn
m_axis_aclk
m_src_axi
m_axis
irq
m_axis_xfer_req
ADI AXI DMA Controller
sys_ps7
GMII_ETHERNET_0
MDIO_ETHERNET_0
GPIO_0
GPIO_I[12:0]
GPIO_O[12:0]
GPIO_T[12:0]
DDR
FIXED_IO
UART_0
SPI_0
SPI0_SCLK_O
SPI0_MOSI_O
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_CLK1
FCLK_RESET0_N
S_AXI_HP0_FIFO_CTRL
S_AXI_HP0
ENET0_EXT_INTIN
M_AXI_GP0_ACLK
S_AXI_HP0_ACLK
IRQ_F2P[15:0]
ZYNQ
ZYNQ7 Processing System
ttc0_wave1_out
GMII
MDIO_PHY
gpio_o[12:0]
gpio_t[12:0]
ddr
fixed_io
UART_0
lcd_scl
lcd_sda
ttc0_wave0_out
clk_25m
sys_rstgen
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
GND_1
dout[0:0]
Constant
sys_concat_intc
In0[0:0]
In1[0:0]
In2[0:0]
In3[0:0]
In4[0:0]
In5[0:0]
In6[0:0]
In7[0:0]
In8[0:0]
In9[0:0]
In10[0:0]
In11[0:0]
In12[0:0]
In13[0:0]
In14[0:0]
In15[0:0]
dout[15:0]
Concat
hdmi_generator_0
s_axis_rgb
reset_100m
clk_100m
cx[9:0]
cy[9:0]
screen_width[9:0]
screen_height[9:0]
pixel_reset
pixel_clk
pixel_x5_clk
rgb[23:0]
hdmi_generator_v1_0
hdmi_0
clk_pixel_x5
clk_pixel
clk_audio
reset
rgb[23:0]
audio_sample_word_0[15:0]
audio_sample_word_1[15:0]
tmds_0
tmds_1
tmds_2
tmds_clock
cx[9:0]
cy[9:0]
frame_width[9:0]
frame_height[9:0]
screen_width[9:0]
screen_height[9:0]
hdmi_v1_0
audio_sample_word_GND
dout[15:0]
Constant
hdmi_d0
hdmi_d1
hdmi_d2
hdmi_clk
gpio_i[12:0]